A DUAL-GATE FET CONSTANT PHASE VARIABLE POWER AMPLIFIER

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ABSTRACT

A 1-Watt X-band variable power amplifier is described which employs an 1800 μm GaAs dual-gate FET. Small-signal models of the device are presented and used to design for minimum insertion phase change over the gain control range. The amplifier has a power-added efficiency of 25 percent and its insertion phase varies less than 15 degrees over a 15 dB gain control range.

INTRODUCTION

Numerous small-signal amplifiers employing the dual-gate GaAs MESFET have been reported in the literature. The device has shown potential for higher gain than its single-gate counterpart and this gain can be reduced up to 30 dB by reducing the second gate voltage. The dual-gate FET is also useful as a variable power amplifier (VPA).

Many applications require that insertion phase remain constant as the power is reduced. This problem is considered here, both analytically and experimentally.

DUAL-GATE FET MODELING

Figure 1 is a photograph of the 1 W power dual-gate FET (DGFET). The total channel width is 1800 μm. Each gate length is 0.5 μm. Gate-1 to source, gate-1 to gate-2, and gate-2 to drain spacings are all 1.5 μm. Source terminals are via grounded. The gate-2 terminals are left unterminated for modeling and design flexibility. Gate-2 can be RF shorted with short bond wires connected to the on-chip 10 pF bypass capacitors.

The dual-gate FET (DGFET) is modeled as a cascode connection of two single-gate FETs [1]. Gate-1 is used as the input, gate-2 is RF terminated and the drain (drain-2) is used as the output. The drain and gate-1 voltages are fixed. Gate-2 voltage is varied to effect gain control.

The gain control mechanism is readily understood by examining how the internal bias conditions vary with gate-2 voltage. Tsironis [1] proposed a graphical technique for determining internal bias conditions which is reproduced as Figure 2. The bottom axis represents Vds1 and the top axis represents Vds2. This example is for a Vd2 of 8 V. (Vds1 + Vds2 = 8 V). The FET1 contours (solid lines) are the familiar constant Vg1, Id1 versus Vd1 contours. The FET2 contours (dashed lines) are constant Vg2, Id2 versus Vs2 contours for Vd2 = 8 V. The operating point is the intersection of the solid curve corresponding to the gate-1 bias and the dashed curve corresponding to the gate-2 bias, since Vs2 = Vd1 and Id2 = Id1.

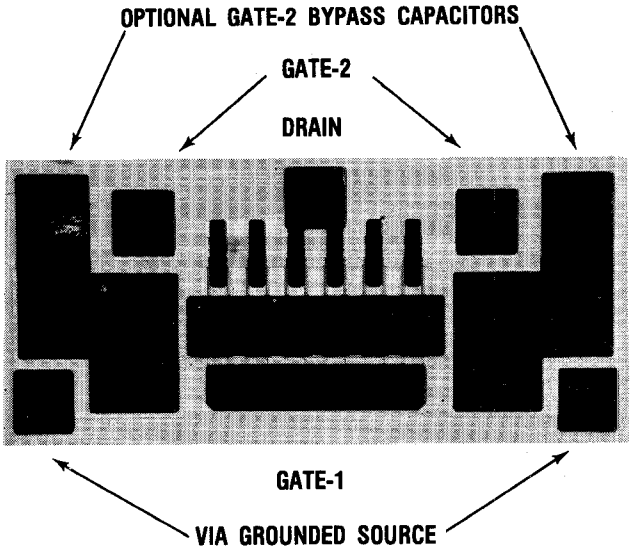

Figure 1. Photograph of the Experimental 1800 μm Dual-Gate FET.

The variable gain operating point traverses a constant gate-1 contour. For a positive gate-2 voltage (i.e., +1V), both FETs are operating in their saturated current regions. This is the maximum gain condition. As the gate-2 voltage is decreased,

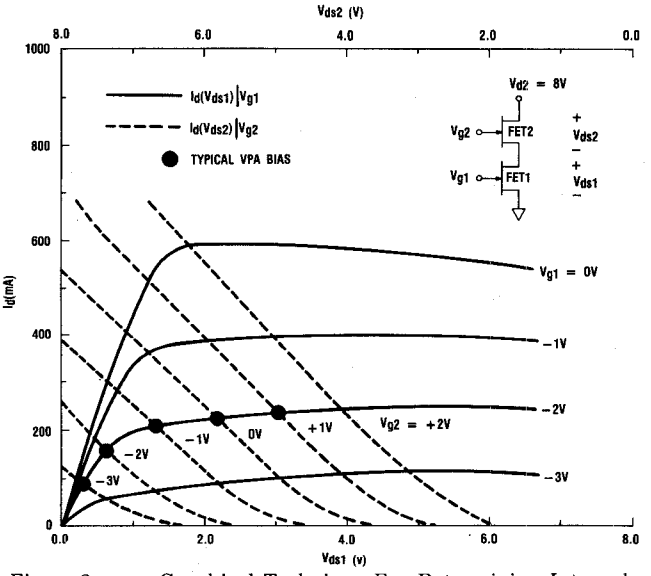

Figure 2. Graphical Technique For Determining Internal Bias Conditions (After Tsironis).

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FET1 moves into the non-saturated current region. In this region, Gm1 begins to decrease and Rds1 decreases drastically. The decrease in Gm1 decreases the signal current available from FET1. And the decrease in Rds1 causes less of this signal current to flow through FET2 to the output.

In order to better understand DGFET variable power amplifier operation, a set of small-signal models was generated. Gate-1 and drain-2 bias levels were selected to optimize power and efficiency (determined in an independent experiment). Three-port S-parameters were measured from 2 - 12 GHz at eight gate-2 voltages covering the useful gain control range of the device.

Element values for the model topology shown in Figure 3 were chosen to fit the measured S-parameters. A typical fit is illustrated in the plots of Figure 4. Table 1 lists the element values versus gate-2 voltage for typical variable power amplifier bias conditions. Using the results from Table 1, a polynomial function of Vg2 was generated for each element value so the device could by analyzed for any gate-2 voltage.

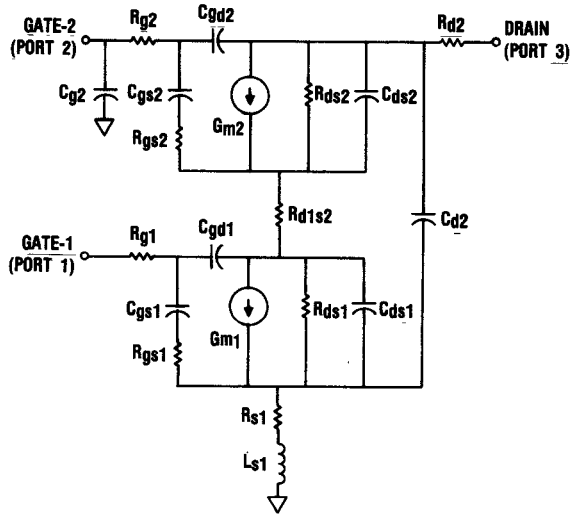
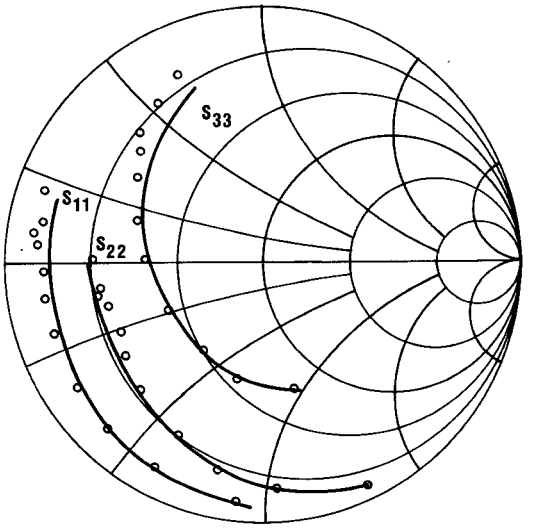


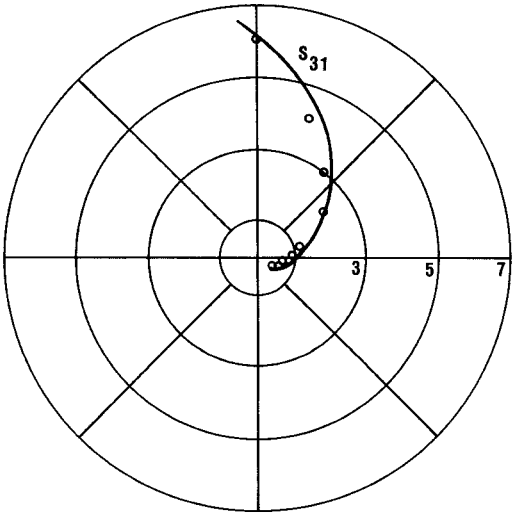
Figure 3. Dual-gate FET Small-Signal Model.

Table 1. Dual-Gate FET Model Element Values Versus Gate-2 Voltage.

Vg2 (V)		+1.5	+1.0	+0.5	+0.0	-1.0	-2.0	-3.0	-4.0
BIAS:									
Vds1	(V)	3.4	2.9	2.4	1.9	1.1	0.7	0.4	0.2
Vds2	(V)	4.6	5.1	5.6	6.1	6.9	7.3	7.6	7.6
Vgs1	(V)	-1.9	-1.9	-1.9	-1.9	-1.9	-1.9	-1.9	-1.9
Vgs2	(V)	-1.9	-1.9	-1.9	-1.9	-2.1	-2.7	-3.4	-4.2
Id	(mA)	308	304	301	297	285	245	164	91
FET1:									
Cds1	(fF)	160	160	160	160	160	160	160	160
Cgs1	(fF)	1260	1210	1200	1150	1070	1140	1070	1060
Cgd1	(fF)	97	112	121	139	185	230	249	262
Gm1	(mS)	161	167	172	171	179	154	77	55
Rds1	(Ω)	28.9	27.5	26.7	23.8	15.7	3.3	1.7	1.1
Rgs1	(Ω)	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1
FET2:									
Cds2	(fF)	160	160	160	160	160	160	160	160
Cgs2	(fF)	1260	1310	1360	1350	1390	1340	1220	980
Cgd2	(fF)	97	97	97	97	97	97	97	97
Gm2	(mS)	161	160	160	159	161	151	127	91
Rds2	(Ω)	28.9	28.1	27.9	30.7	32.2	38.1	36.6	38.6
Rgs2	(Ω)	1.2	1.2	1.2	1.2	1.2	1.3	1.3	1.4
Cd2 = 350 fF Cg2 = 150 fF τ = 1.4 ps				Rd2 = 0.6 ohm Rg1 = 1.8 ohm Rg2 = 1.9 ohm		Rd1s2 = 0.8 ohm Rs1 = 0.5 ohm Ls1 = 0.03 nH			



(a) S11, S22, S33



(b) S31

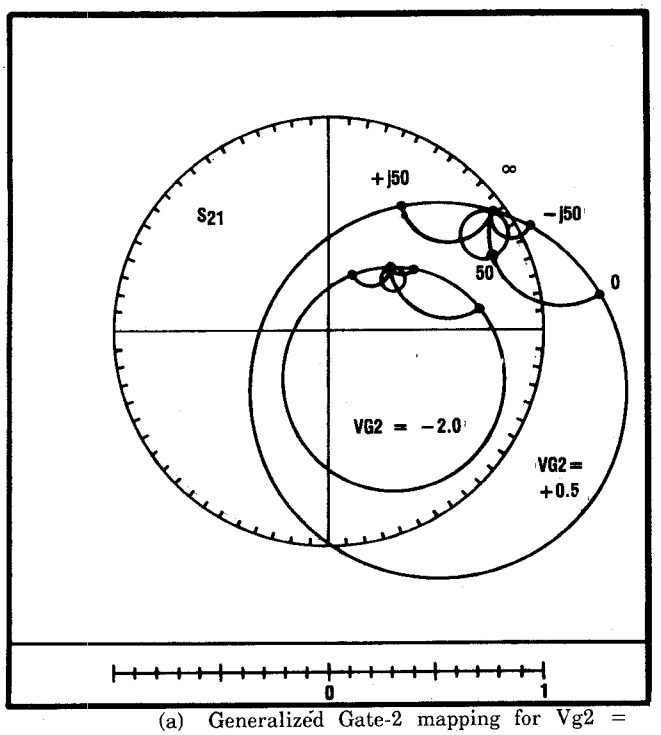
Figure 4. Modeled versus Measured S-parameters Illustrating a Typical Fit.

DESIGN

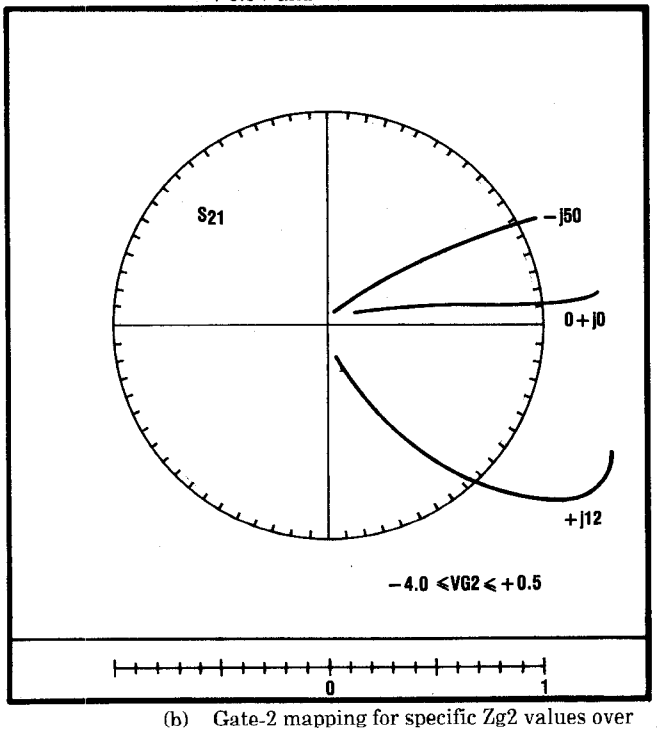
A single-stage dual-gate FET power amplifier was designed for X-band operation using a TI 1800 μm DGFET. The gain and output power can be controlled by varying the second gate voltage. The objective of this design was to achieve an amplitude control of 15 to 20 dB while minimizing insertion phase variation.

The dual-gate FET is transformed into a two-port network by terminating the second gate with an impedance Zg2. This configuration is a cascode circuit with a common-source input stage driving a common-gate output stage with series feedback. The mathematical transformations for converting the scattering parameters of a three-port device to a two-port device with the third port terminated have been derived by Bodway [2]. Using these relationships, the dependence of gain, phase, and stability on the second gate termination can be determined and have been reported by Pengelly [3] and Liechti [4].

Figure 5 graphically demonstrates the effect of the second gate termination on the forward transfer characteristic of an 1800 µm DGFET. In Figure 5(a) loci of gate-2 terminating impedances (indicated as the distorted Smith Chart) are mapped onto the S21 plane at a single frequency. Mappings for gate-2 voltages of +0.5 and -2.0 volts are indicated.



(a) Generalized Gate-2 mapping for Vg2 = +0.5V and -2.0V.



(b) Gate-2 mapping for specific Zg2 values over Vg2 bias range.

Figure 5. Mapping of Gate-2 Termination Impedance (Zg2) Onto the S21 Plane.

A comparison of these two mappings shows that the insertion phase of the device is quite sensitive to inductive terminations, while capacitive terminations provide less phase variation. This is more clearly indicated in Figure 5(b) where specific termination impedances of -j50, 0, and +j12 ohms are mapped onto the S21 plane for a continuous range of gate-2 voltage.

Inductive terminations yield maximum gain, but can also lead to potentially unstable devices. The optimum termination impedance is one which yields sufficient maximum gain with minimum phase change as the gain is reduced. This termination tends to be near the RF short circuit condition and may be different at each frequency. This mapping demonstrates 13 degrees of phase shift for 16 dB of gain reduction for the short circuit condition on gate-2.

Utilizing mappings at various frequencies, the second gate matching circuit can be designed for optimum phase and gain control. For relatively narrow-band applications, simple inductive or capacitive loading is sufficient. Broad-band applications would require the synthesis of a matching network providing an optimum impedance versus frequency characteristic. In this design, a slightly inductive termination was selected and implemented using a series resonant L-C circuit. Analysis of this design demonstrated less than 7 degrees of phase variation for a minimum of 15 dB of gain control over a 10 percent bandwidth. The input matching network consists of a lumped low-pass filter and series resistor for low frequency stability. The output network is a load-line derived quarter-wave matching network for optimum power transfer. A photograph of the assembled hybrid circuit is shown in Figure 6.

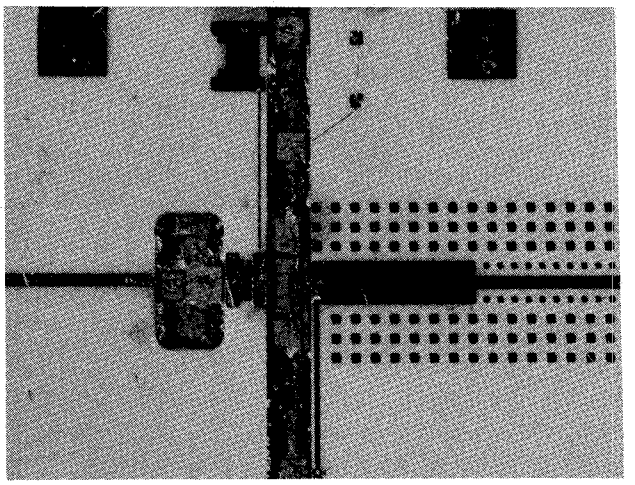


Figure 6. Photograph of the Experimental Variable Power Amplifier.

PERFORMANCE

Figure 7 shows measured gain and power performance versus frequency for a saturated drive condition. It also illustrates the measured gain/power control response of the circuit. Notice that gain flatness is maintained throughout the 18 dB gain control range. An output power level of 29.0 dBm (0.8 W) at 10.0 GHz is recorded in Table 2. This operating point yields 6.0 dB of gain over a 10 percent, 1 dB bandwidth with a corresponding power added efficiency of 25 percent. A typical TI 1500 µm single-gate FET circuit delivers 28 dBm of power with 6.0 dB gain and 29 percent power added efficiency.

VPA gain performance curves versus gate-2 voltage are plotted in Figure 8 for small-signal and saturated drive levels.

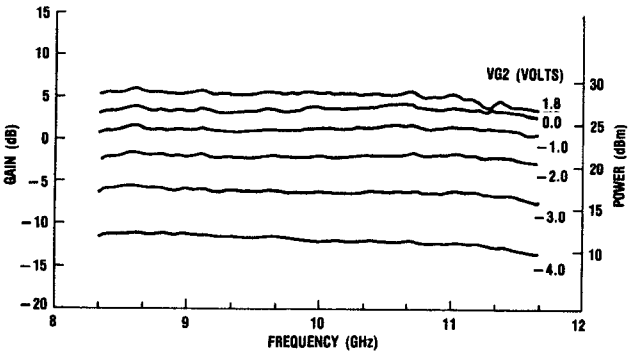


Figure 7. Gain at Peak Efficiency Versus Frequency of the Variable Power Amplifier.

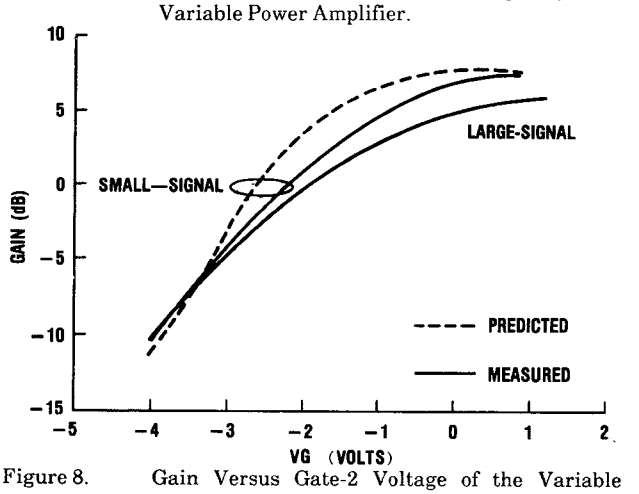


Figure 8. Gain Versus Gate-2 Voltage of the Variable Power Amplifier (50% Duty Cycle, Center Frequency).

Notice the excellent agreement of the measured and predicted small-signal responses. These responses are within 0.3 dB at the maximum gain condition and within 2 dB elsewhere in the range.

Insertion phase variations are plotted with respect to gain control in Figure 9. Each response is normalized to its maximum gain. For 15 dB of gain reduction under small-signal conditions, 7.1 degrees of measured phase variation is compared to 5.0 degrees predicted by the model. Saturated conditions demonstrated 15 degrees of phase variation for the same gain reduction.

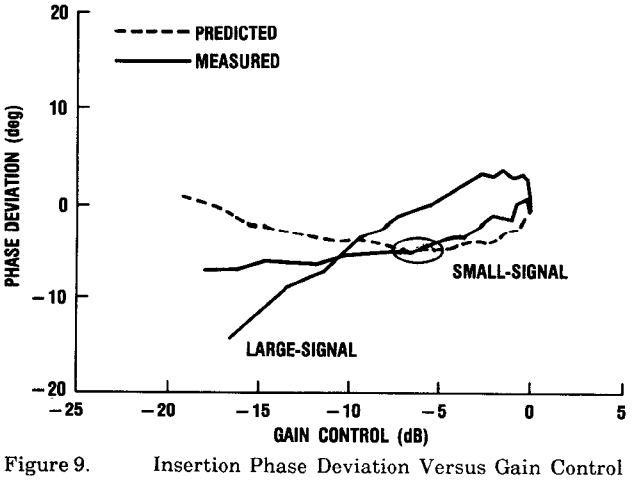


Figure 9. Insertion Phase Deviation Versus Gain Control of the Variable Power Amplifier.

Table 2. Performance Summary of the Variable Power Amplifier.

	SMALL-SIGNAL	PEAK EFFICIENCY	SATURATED
MAXIMUM GAIN	7.6 dB	6.0 dB	4 0 dB
MAXIMUM POWER	--	29.0 dBm	30.0 dBm
POWER ADDED EFFICIENCY	--	25%	24%
GAIN/POWER CONTROL RANGE	15 dB	15 dB	15 dB
ASSOCIATED PHASE CHANGE	7	15	25

CONCLUSION

A small-signal model for an 1800 μm dual-gate FET has been developed and discussed. Using this model, a design technique has been presented for designing a variable power amplifier where control of insertion phase is an important consideration. Amplitude and phase characteristics of a 1-watt VPA have been measured and compared with theory.

ACKNOWLEDGEMENT

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REFERENCES

[1] C. Tsironis, R. Meierer, "Microwave Wide-Band Model of GaAs Dual Gate MESFET's," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp. 243-251, March 1982.

[2] G.E. Bodway, "Circuit Design and Characterization of Transistors by Means of Three-port Scattering Parameters," Microwave J., vol. 11, pp. 55-63, May 1968.

[3] R.S. Pengelly, Microwave Field-Effect Transistors - Theory, Design and Applications. London: Research Studies Press Division of John Wiley and Sons Ltd., 1982.

[4] C.A. Liechti, "Performance of Dual-Gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," IEEE Trans. Microwave Theory Tech., vol. MTT-23, pp. 461-469, June 1975.